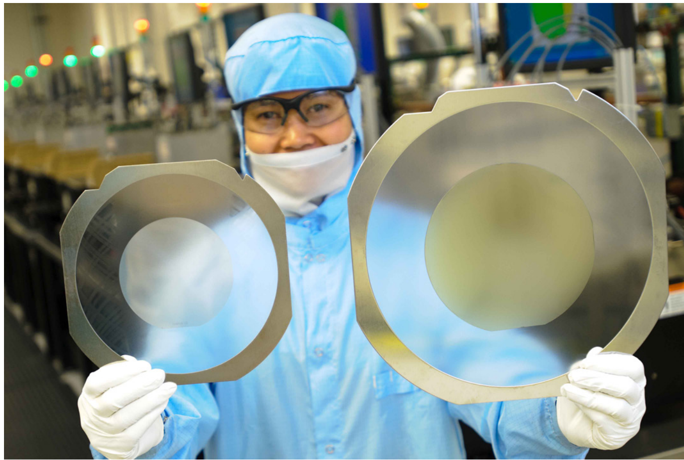
CREE®

Cree Silicon Carbide Substrates and Epitaxy



Supported diameters:

◇ 76.2 mm

◇ 100.0 mm

◇ 150.0 mm

Product Specifications

4H Silicon Carbide Substrates
N-type, P-type, and Semi-Insulating

N-type and P-type Silicon Carbide Epitaxy

Cree® is the global leader in the manufacture of 4H silicon-carbide (SiC) substrates, SiC and III-Nitride epitaxial wafers.

The Materials Business Unit produces a wide assortment of conductive and semi-insulating products ranging in wafer diameters up to 150.0 mm. This material is the foundation for Cree's vertically-integrated structure and is manufactured upon a high-volume platform process that provides our customers the highest degree of material **quality**, **supply assurance**, and **economies of scale**.

Product applications include:

4H-N SiC Substrates/SiC Epitaxy

- Optoelectronics
- Power-factor correction
- Solar inverters
- Industrial motor drives

4H-HPSI SiC Substrates/III-Nitride Epitaxy

- High-power RF
- Graphene
- Terahertz

To learn more, visit www.cree.com/materials

Physical Properties

Polytype	Single-Crystal 4H
Crystal structure	Hexagonal
Bandgap	3.26 eV
Thermal conductivity (n-type; 0.020 ohm-cm)	a~4.2 W/cm • K @ 298 K c~3.7 W/cm • K @ 298 K
Thermal conductivity (HPSI)	a~4.9 W/cm • K @ 298 K c~3.9 W/cm • K @ 298 K
Lattice parameters	a=3.073 Å c=10.053 Å
Mohs hardness	~9

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76.2 and 100.0 mm SiC Substrate Product Descriptions

Part Number / **Options**

W X X X X X X – X X X X

- X (12th) → 0 = no epitaxy; 1 = 1 layer; 2 = 2 layers; 3 = 3 layers; 4 = 4 layers; 5 = 5 layers
- X (11th) → 0 = no epitaxy; S = standard SiC epitaxy; T = thick SiC epitaxy
- X (10th) → 2 = double-side polish, Si-face CMP, epi ready; 6 = double-side polish, C-face CMP, epi ready
- X (9th) → 0 = standard micropipe; B = low basal plane dislocation density (BPD)*; L = low micropipe; V = very-low micropipe; U = ultra-low micropipe; Z = zero micropipe (ZMP™)
- X (7th) → resistivity code (see appropriate specification sheet)
- X (6th) → 0 = on-axis; 4 = 4.0° off-axis; 8 = 8.0° off-axis
- X (5th) → E = 76.2 mm (3.0”); F = 100.0 mm
- X (4th) → P = production-grade; R = research-grade
- X (3rd) → N = N-type; P = P-type; T = high-purity semi-insulating
- X (2nd) → 4 = 4H
- W → W = standard product

* Low basal plane dislocation material is available for 100-mm diameter substrates only

See page 9 for 150-mm product descriptions

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76.2 mm SiC Substrate Product Descriptions

Part Number	Type	Orientation	Micropipe Density	Resistivity Ohm-cm Range	Bin
N-Type Low Micropipe Density					
W4NxE4C-L200	N	4° Off	≤15 micropipes/cm²	0.015-0.028	C
W4NxE8C-L200	N	8° Off	≤15 micropipes/cm²	0.015-0.028	C
N-Type Very-Low Micropipe Density					
W4NxE4C-V200	N	4° Off	≤5 micropipes/cm²	0.015-0.028	C
W4NxE8C-V200	N	8° Off	≤5 micropipes/cm²	0.015-0.028	C
N-Type Ultra-Low Micropipe Density					
W4NxE4C-U200	N	4° Off	≤1 micropipes/cm²	0.015-0.028	C
W4NxE8C-U200	N	8° Off	≤1 micropipes/cm²	0.015-0.028	C
N-Type Zero Micropipe Density (ZMP™)					
W4NxE4C-Z200	N	4° Off	0 micropipes/cm²	0.015-0.028	C
N-Type LCW					
W4NRE0X-0200	N	On-axis	N/A	0.013-2.000	N/A
P-Type					
W4PRE8F-0200	P	8° Off	N/A	≤2.5	F
High-Purity Semi-Insulating					
W4TRE0R-0200	HPSI	On-axis	N/A	≥ 1E5	R
W4TRE8R-0200	HPSI	8° Off	N/A	≥ 1E5	R

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100.0 mm SiC Substrate Product Descriptions

Part Number	Type	Orientation	Micropipe Density	Resistivity Ohm-cm Range	Bin
N-Type Low Micropipe Density					
W4NxF4C-L200	N	4° Off	≤15 micropipes/cm²	0.015-0.028	C
N-Type Very-Low Micropipe Density					
W4NxF4C-V200	N	4° Off	≤5 micropipes/cm²	0.015-0.028	C
N-Type Ultra-Low Micropipe Density					
W4NxF4C-U200	N	4° Off	≤1 micropipes/cm²	0.015-0.028	C
W4NxF4C-B200	N	4° Off	≤1 micropipes/cm²	0.015-0.028	C, BPD ≤1,000/cm²
N-Type Zero Micropipe Density (ZMP™)					
W4NxF4C-Z200	N	4° Off	0 micropipes/cm²	0.015-0.028	C
N-Type LCW					
W4NRF0X-0200	N	On-axis	N/A	0.013-2.000	N/A
High-Purity Semi-Insulating					
W4TRF0R-0200	HPSI	On-axis	N/A	≥1E5	R

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Dimensional Properties, Terminology and Methods

Diameter
The linear dimension across the surface of a wafer. Measurement is performed manually with ANSI-certified digital calipers on each individual wafer (see Figure 1).

Thickness, center point
Measured with ANSI-certified non-contact tools at the center of each individual wafer.

Flat length
Linear dimension of the flat measured with ANSI-certified digital calipers on a sample of one wafer per ingot (see Figure 1).

Surface orientation
Denotes the orientation of the surface of a wafer with respect to a crystallographic plane within the lattice structure. In wafers cut intentionally "off orientation," the direction of cut is parallel to the primary flat, away from the secondary flat. Measured with x-ray goniometer on a sample of one wafer per ingot in the center of the wafer.

Orthogonal misorientation
In wafers cut intentionally "off orientation," the angle between the projection of the normal vector to the wafers surface onto a {0001} plane and the projection on that plane of the nearest <1120> direction.

Primary flat
The primary flat is the {1010} plane with the flat face parallel to the <1120> direction.

Primary flat orientation
The flat of the longest length on the wafer, oriented such that the chord is parallel with a specified low-index crystal plane. Measured on one wafer per ingot using Laue back-reflection technique with manual angle measurement.

Secondary flat orientation
A flat of shorter length than the primary orientation flat, whose position with respect to the primary orientation flat identifies the face of the wafer.

Marking
For silicon-face-polished material, the carbon face of each individual wafer is laser-marked with OCR-compatible font, similar to definitions and characteristics in SEMI M12 (see Figure 1). For carbon-face-polished material, the silicon face of each individual wafer is laser-marked (see Figure 2). 150.0 mm substrates have no secondary flat, and the marking convention is identical to that of 76.2 and 100 mm products.

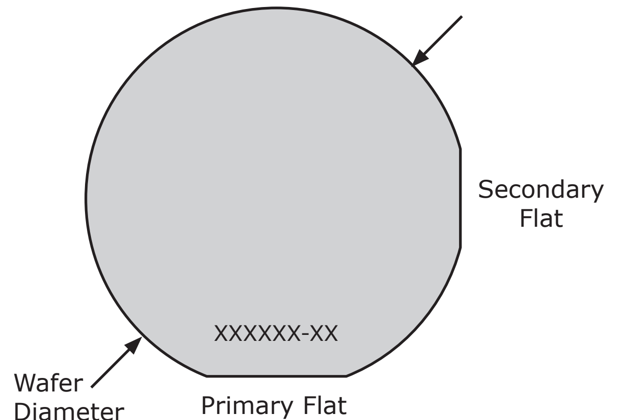

Figure 1. Diameter, primary and secondary flat locations, and marking orientation, carbon face up for silicon face polished wafers

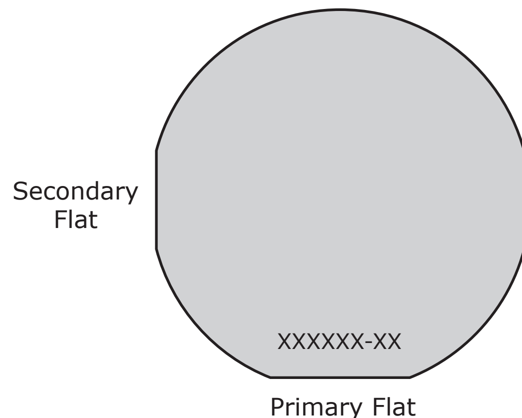

Figure 2. Primary and secondary flat locations, and marking orientation, silicon face up for carbon face polished wafers

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76.2 mm SiC Substrate Specifications

Substrate Property	Cree Standard
Diameter	3.000″ ± 0.015″ 76.2 mm ± 0.38 mm
Thickness N-type on-axis	0.0145″ ± 0.0025″ 368.0 µm ± 64.0 µm
Thickness N-type off-axis; semi-insulating	0.0138″ ± 0.001″ 350.0 µm ± 25.0 µm
Dopant	n-type: Nitrogen
Primary flat length	0.875″ ± 0.125″ 22.22 mm ± 3.17 mm
Secondary flat length	0.440″ ± 0.060″ 11.18 mm ± 1.52 mm
Surface orientation on-axis	{0001} ± 0.25°
Surface orientation off-axis	4.0° toward <1120> ± 0.5° 8.0° toward <1120> ± 0.5°
Surface finish	Both sides polished
Orthogonal misorientation	± 5.0°
Primary flat orientation	<1120> ± 5.0°
Secondary flat orientation	90.0° CW from Primary ± 5.0°, silicon face up
TTV	≤15 microns, full substrate
Warp	≤35 microns, full substrate
LTV (average, 1 cm^2 site)	≤4 microns, full substrate
Packaging	Multi-wafer box unless otherwise specified

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100.0 mm SiC Substrate Specifications

Substrate Property	Cree Standard
Diameter	100.0 mm +0.0/-0.5 mm
Thickness N-type on-axis	500.0 µm ± 50.0 µm
Thickness N-type off-axis	350.0 µm ± 25.0 µm
Thickness Semi-insulating	500.0 µm ± 25.0 µm
Dopant	n-type: nitrogen
Primary flat length	32.5 mm ± 2.0 mm
Secondary flat length	18.0 mm ± 2.0 mm
Surface orientation On-axis	{0001} ± 0.25°
Surface orientation Off-axis	4.0° toward <1120> ± 0.5°
Surface finish	Both sides polished
Orthogonal misorientation	± 5.0°
Primary flat orientation	<1120> ± 5.0°
Secondary flat orientation	90.0° CW from primary ± 5.0°, silicon face up
TTV	≤15 microns, full substrate
Warp	≤45 microns, full substrate
LTV (average, 1 cm^2 site)	≤4 microns, full substrate
Packaging	Multi-wafer box unless otherwise specified

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150.0 mm SiC Substrate Product Descriptions

Part Number **Options**

W X X X X X X – X X - X X X X

- 0 = no epitaxy
- 1 = 1 layer
- 2 = 2 layers
- 3 = 3 layers
- 4 = 4 layers
- 5 = 5 layers

- 0 = no epitaxy
- S = standard epitaxy
- T = thick epitaxy

- 2 = double-side polish, Si-face CMP, epi ready
- 6 = double-side polish, C-face CMP, epi ready

- V = very-low micropipe
- U = ultra-low micropipe

- None = 500-µm thickness
- 1 = 350-µm thickness

C

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resistivity code
(see appropriate specification sheet)

- 0 = on-axis
- 4 = 4.0° off-axis

G = 150.0 mm (6.0”)

- P = production grade
- R = research grade

- N = N-type
- T = high-purity semi-insulating

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4 = 4H

W = standard product

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150.0 mm SiC Substrate Product Descriptions

Part Number	Type	Orientation	Micropipe Density	Resistivity Ohm-cm Range	Bin
N-Type Very-Low Micropipe Density					
W4NRG4C-C_x-V200	N	4° Off	≤5 micropipes/cm^2	0.015-0.028	C
N-Type Ultra-Low Micropipe Density					
W4NPG4C-C_x-U200	N	4° Off	≤1 micropipes/cm^2	0.015-0.028	C
High-Purity Semi-Insulating					
W4TRG0R-C_x-0200	HPSI	On-axis	N/A	>1E5	R

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150.0 mm SiC Substrate Specifications

Substrate Property	Cree Standard	
Diameter	5.905” ± 0.984” 150.0 mm ± 0.25 mm	
Thickness N-type on-axis; semi-insulating	n-type: TBD HPSI: 500 µm ± 25 µm	
Thickness N-type off-axis; semi-insulating	C specification: 500 µm ± 25 µm C1 specification: 350 µm ± 25 µm	
Dopant	n-type: nitrogen	
Primary flat length	1.870” ± 0.059” 47.5 mm ± 1.5 mm	
Secondary flat length	none	
Surface orientation on-axis	{0001} ±0.25°	
Surface orientation off-axis	4.0° toward <11-20> ± 0.5°	
Surface finish	Si-face CMP polish, C-face optical polish C-face CMP polish, Si-face optical polish	
Orthogonal misorientation	± 5.0°	
Primary flat orientation	<11-20> ± 5°	
Secondary flat orientation	N/A	
	N-type	HPSI
TTV	Production-grade: ≤10 µm Research-grade: ≤10 µm	Research-grade: <10 µm
Warp	Production-grade: ≤40 µm Research-grade: ≤60 µm	Research-grade: <60 µm
LTV (average, 1 cm^2 site)	Production-grade: ≤2 µm Research-grade: ≤4 µm	Research-grade: ≤4 µm
Edge chips by diffuse lighting	Production-grade: none permitted Research-grade: qty. 2 ≥1.0 mm width and depth	Research-grade: 2 ≤1.0 mm width & depth

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Standard Specifications for Polished SiC Substrates - Surface Finish

76.2, 100.0 and 150.0 mm SiC Substrates

Characteristics	Production-Grade	Research-Grade
Edge chips/indents by diffuse lighting†	none permitted	2 ≤1.0 mm width & depth
Orange peel/pits by diffuse lighting*Δ	≤10% area	≤30% area
Striations by diffuse lighting	3 allowed ≤3 mm each	20 allowed ≤7 mm each
Polytype areas by diffuse lighting*	≤5% area	≤20% area
Area contamination (stains) by high-intensity light	none permitted	none permitted
Cracks by high-intensity light	none permitted	none permitted
Hex plates by high-intensity light*	cumulative area ≤10%	cumulative area ≤30%
Scratches by high-intensity light*	5 scratches to 1X wafer diameter cumulatvie length	8 scratches to 1.5X wafer diameter cumulatvie length
Masking defects (mounds)* Quantitative by 200X microscopic inspection	10 defects in 3 or less of the 9 fields inspected in a cross pattern	10 defects in 5 or less of the 9 fields inspected in a cross pattern
Contamination Quantitative by 200X microscopic inspection	none in inspected fields	none in inspected fields
Cumulative area defects* Quantitative by 200X microscopic inspection	≤10% area	≤30% area

Notes:
* Defect limits apply to entire wafer surface except for edge exclusion area, which is 2 mm for 76.2 mm substrates and 3 mm for 100.0 and 150.0 mm substrates.
◊ Pits must be <2 mm in distance from one another to be considered a reject cause.
† Edge chips must be >0.5 mm on R-grade material to be considered a reject cause.

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Terminology and Methods for Polished SiC Substrates – Surface Finish

(Area) Contamination
Any foreign matter on the surface in localized areas which is revealed under high-intensity (or diffuse) illumination as discolored, mottled, or cloudy appearance resulting from smudges, stains or water spots.

Cracks
A fracture or cleavage of the wafer that extends from the frontside surface of the wafer to the back-side surface of the wafer. Cracks must exceed 0.010” in length under high-intensity illumination in order to discriminate fracture lines from allowable crystalline striations. Fracture lines typically exhibit sharp, thin lines of propagation, which discriminate them from material striations.

Edge chips
Any edge anomalies (including wafer-saw exit marks) in excess of 1.0 mm in either radial depth or width. As viewed under diffuse illumination, edge chips are determined as unintentionally missing material from the edge of the wafer.

Edge exclusion
The outer annulus of the wafer is designated as wafer handling area and is excluded from surface finish criteria (such as scratches, pits, haze, contamination, craters, dimples, grooves, mounds, orange peel and saw marks). This annulus is 2 mm for 76.2 mm substrates, and 3 mm for 100.0 mm substrates.

Hex plate
Hexagonal-shaped platelets on the surface of the wafer which appear silver in color to the unaided eye, under diffuse illumination.

Masking defects (also referred to as “Mound”)
A distinct raised area above the wafer frontside surface as viewed with diffuse illumination.

Orange peel
Visually detectable surface roughening when viewed under diffuse illumination.

Pits
Individual distinguishable surface anomalies, which appears as a depression in the wafer surface with a length-to-width ratio less than 5 to 1, and visible under high-intensity illumination.

Foreign polytypes (also referred to as “Inclusions” or “Crystallites”)
Regions of the wafer crystallography which are polycrystalline or of a different polytype material than the remainder of the wafer, such as 6H mixed in with a 4H type substrate. Foreign polytype regions frequently exhibit color changes or distinct boundary lines, and are judged in terms of area percent under diffuse illumination.

Scratches
A scratch is defined as a singular cut or groove into the frontside wafer surface with a length-to-width ratio of greater than 5 to 1, and visible under high-intensity illumination.

Striations
Striations in silicon carbide are defined as linear crystallographic defects extending down from the surface of the wafer which may or may not pass through the entire thickness of the wafer, and generally follow crystallographic planes over its length.

Total usable area
A cumulative subtraction of all noted defect areas from the frontside wafer quality area within the edge exclusion zone. The remaining percent value indicates the proportion of the frontside surface to be free of all noted defects (does not include edge exclusion).

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Specifications for SiC Epitaxial Wafers - 76.2, 100.0 and 150.0 mm Substrates

Substrate Orientation: Epitaxy is available only for off-axis substrates		
Conductivity	n-type	p-type
Dopant	Nitrogen	Aluminum
Net doping density	N_D-N_A	N_A-N_D
Silicon face	9E14 – 1E19/cm^3	9E14 – 1E19/cm^3
Carbon face	1E16 – 1E19/cm^3	Not available
Tolerance	±25%	±50%
Thickness range – silicon face		
0.2–50.0 microns	±10% of selected thickness	±10% of selected thickness
Thickness range – carbon face		
0.2–1.0 microns	±25% of selected thickness	Not available
1.0–10.0 microns	±15% of selected thickness	Not Available

Notes:

- 2 mm edge exclusion for 76.2 mm, 3 mm edge exclusion for 100.0 and 150.0 mm
- N-type epi layers <20 microns are preceeded by n-type, 1E18, 0.5 micron buffer layer
- N-type epi layers ≥20 microns are preceeded by n-type, 1E18, 1.0 micron buffer layer
- No buffer layer for p-type epitaxial layers
- Not all doping densities are available in all thicknesses
- Contact Cree Sales for specifications on multi-layer or unique epitaxy requests

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Specifications for SiC Epitaxial Wafers - 76.2, 100.0 and 150.0 mm Substrates

<table>
<tr><th>Characteristics</th><th colspan="2">Maximum Acceptability Limits</th><th>Test Methods</th><th>Defect Definitions (see pg. 14)</th><th>Methodology (see pg. 15)</th></tr>
<tr><td rowspan="3">Large-point defects</td><td>76.2 mm</td><td>30</td><td rowspan="10">Diffuse illumination</td><td rowspan="3">D1</td><td rowspan="7">M1, M2</td></tr>
<tr><td>100.0 mm</td><td>40</td></tr>
<tr><td>150.0 mm</td><td>50</td></tr>
<tr><td>Scratches</td><td colspan="2">10 lines <2x wafer diameter</td><td>D2</td></tr>
<tr><td>Dimpling</td><td colspan="2"><5% affected</td><td>D3</td></tr>
<tr><td rowspan="2">Step bunching</td><td>4.0° off-axis</td><td>N/A</td><td rowspan="2">D4</td></tr>
<tr><td>8.0° off-axis</td><td><10% affected</td></tr>
<tr><td>Backside cleanliness</td><td colspan="2">95% clean</td><td>D5</td></tr>
<tr><td>Edge chips</td><td colspan="2">2 with radius 1.5 mm</td><td>D6</td><td rowspan="3">M2</td></tr>
<tr><td>ID correct/legible</td><td colspan="2">Yes</td><td rowspan="2">D7</td></tr>
<tr><td>Wafer flats</td><td colspan="2">Yes</td></tr>
<tr><td>Epi defects</td><td colspan="2">25/cm^2</td><td>Microscopic</td><td>D8-D12</td><td>M3</td></tr>
<tr><td>Net doping</td><td colspan="2">See specification table</td><td>Hg probe CV</td><td>–</td><td>M4</td></tr>
<tr><td>Thickness</td><td colspan="2">See specification table</td><td>FTIR</td><td>–</td><td>M5</td></tr>
</table>

Notes:

- 2 mm edge exclusion for 76.2 mm, 3 mm edge exclusion for 100.0 and 150.0 mm

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Definitions

D1. Large-point defects
Defects which exhibit a clear shape to the unassisted eye and are > 50 microns across. These features include spikes, adherent particles, chips and craters. Large point defects less than 3 mm apart count as one defect.

D2. Scratches
Grooves or cuts below the surface plane of the wafer having a length-to-width ratio of greater than 5 to 1. Scratches are specified by the number of discrete scratches times the total length in fractional diameter.

D3. Dimpling
A texture resembling the surface of a golf ball. Specified in % affected area.

D4. Step bunching
Step bunching is visible as a pattern of parallel lines running perpendicular to the major flat. If present, estimate the % of specified area affected.

D5. Backside cleanliness
Verified by inspecting for a uniform color to the wafer backside. Note there is a darker region near the center of some higher doped wafers. Backside cleanliness specified as percent area clean.

D6. Edge chips
Areas where material has been unintentionally removed from the wafer. Do not confuse fractures in epi crown with edge chips.

D7. ID correct and major wafer flat
Both should be readily discernible.

Epitaxy Defects

The sum of discrete microscopic defects counted in specified area. These include 3C inclusions, comet tails, carrots, particles and silicon droplets.

D8. 3C inclusions
Regions where step-flow was interrupted during epi layer growth. Typical regions are generally triangular although more rounded shapes are sometimes seen. Count once per occurrence. Two inclusions within 200 microns count as one.

D9. Comet tails
Comet tails have a discrete head and trailing tail. These features are aligned parallel to the major flat. Usually, all comet tails tend to be of the same length. Count once per occurrence. Two comet tails within 200 microns count as one.

D10. Carrots
Similar to comet tails in appearance except they are more angular and lack a discrete head. If present, these features are aligned parallel to the major flat. Usually, any carrots present tend to be of the same length. Count once per occurrence. Two carrots within 200 microns count as one.

D11. Particles
Particles have the appearance of eyes and if present are usually concentrated at the wafer edges and not within the specified area. If present, count once per occurrence. Two particles within 200 microns count as one.

D12. Silicon droplets
Silicon droplets can appear as either small mounds or depressions in the wafer surface. Normally absent, but if present are largely concentrated at perimeter of wafer. If present, estimate the % of specified area affected.

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Methodology

M1. 2 mm edge exclusion for 76.2 mm, 3 mm edge exclusion for 100.0 and 150.0 mm.

M2. Inspection performed under diffuse illumination.

M3. Microscopic inspection performed at 100X, on an Olympus BH2 UMA Optical Microscope, or comparable. Inspection pattern detailed in Figure 3.

M4. Net doping is determined as an average value of multiple points along radius opposite major flat using Hg probe CV.

M5. Thickness is determined as an average value across the wafer using FTIR, or mass difference.

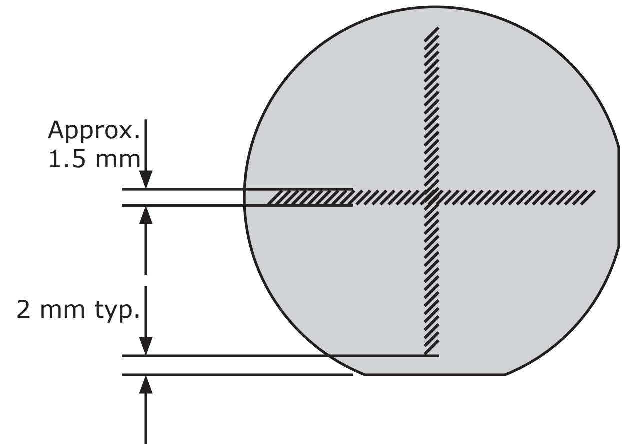

Figure 3. Epi inspection pattern

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